IN THE MATTER OF

KOREAN PATENT APPLICATION

UNDER SERIAL NO. 21139/2003

I, THE UNDERSIGNED, HEREBY DECLARE:

THAT I AM CONVERSANT WITH BOTH KOREAN AND THE ENGLISH LANGUAGES: AND

THAT I AM A COMPETENT TRANSALTOR OF THE APPLICATION PAPERS THE PARTICULARS OF WHICH ARE SET FORTH BELOW:

KOREAN PATENT APPLICATION UNDER

SERIAL NO.: 21139/2003

FILED ON : APRIL 3, 2003

IN THE NAME OF : LG PHILIPS CO., LTD.

FOR : MANUFACTURING METHOD OF LIQUID CRYSTAL DISPLAY DEVICE

IN WITNESS WHEREOF, I SET MY HAND HERETO

THIS 6 TH DAY OF JULY 6, 2006

BY _____

Seong Ok KOH

[Translation]

PATENT APPLICATION

To : Director General

The Patent Office

Date of Application : April 3, 2003

Classification for international patent : G02F 1/333

Title of the Invention : MANUFACTURING METHOD OF LIQUID CRYSTAL DISPLAY DEVICE

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Code No.: 1-1998-101865-5

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Code No.: 9-1998-000202-3

General Authorization registration No.; 1999-055150-5

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This application is hereby filed pursuant to Article 42 of the Patent Law.

/S/ Attorney : PARK, Jang Won

[Translation]

ABSTRACT OF THE DISCLOSURE

A manufacturing method of a thin film transistor of a liquid crystal display device using 3-mask comprises: forming a gate electrode on a substrate; consecutively forming a gate insulating layer and an active layer on the gate electrode; depositing a photoresist on the active layer and performing a photolithography process thus to form a first photoresist pattern, and then removing an active layer formed at a source/drain region; ashing the first photoresist pattern thus to expose a part of an active region; forming a source/drain electrode at the source/drain region; forming a passivation layer on the substrate including the source/drain electrode; forming a second photoresist pattern that exposes a pixel region on the passivation layer; forming a pixel region by using the second photoresist pattern as a mask; side-etching a part of the passivation layer thus to expose a part of the drain electrode; forming a pixel electrode material on the second photoresist pattern and the pixel region; and simultaneously removing the second photoresist pattern and the pixel electrode material formed thereon thus to form a pixel electrode. According to this, processes are simplified and a manufacturing cost is reduced.

[Representative drawing]

Figure 3j

[SPECIFICATION]

[Title of the Invention]

Manufacturing method of liquid crystal display device

[Brief description of the Drawings]

Figures 1A to 1E are views showing manufacturing processes of a thin film transistor of an LCD device using 5-mask in accordance with the conventional art;

Figures 2A to 2H are views showing manufacturing processes of the TFT of an LCD device using 4-mask in accordance with the conventional art; and

Figures 3A to 3I are views showing manufacturing processes of a TFT of an LCD device using 3-mask according to the present invention.

*** Explanations for the major reference numerals ***

300 : substrate	301 : gate electrode
303 : amorphous silicon layer	305 : photoresist
306a : source electrode	306b : drain electrode
307 : passivation layer	308 : photoresist
309 : pixel electrode material	309a : pixel eletrode

[Detailed description of the Invention]

[Object of the Invention]

[Field of the Invention and Background Art]

The present invention relates to a manufacturing process of a thin film transistor used as a switching device of a liquid crystal display device, and more particularly, to a method for reducing the number of masks used at the time of manufacturing a thin film transistor .

Generally, a liquid crystal display (LCD) device is a device for displaying desired information on a screen by controlling an alignment direction of a liquid crystal aligned by an electric field applied between a pixel electrode formed on a TFT array substrate and a common electrode on a color filter. Herein, a thin film transistor is mainly used as a switching device for applying a voltage to the pixel electrode existing on the TFT array substrate.

The number of masks used for manufacturing the LCD device directly affect to the number of processes. The decreased the number of processes is, the increased a productivity and a yield are. According to this, efforts to reduce the number of masks used for manufacturing a thin film transistor have been performed.

Nowadays, a method for manufacturing a TFT by applying 5-mask or 4-mask is mainly used.

Hereinafter, a manufacturing process of a TFT of an LCD device using a general 5-mask will be explained with reference to Figures 1A to 1E.

As shown in Figure 1A, a gate electrode material 11 is formed on a substrate 1. The gate electrode material is a metal material, and is formed by a sputtering method.

The metal layer for forming the gate line also serves as a line of a storage region for maintaining a voltage at a TFT for a predetermined time and a gate pattern of a gate pad portion.

After forming the gate metal layer, a photoresist (not shown) is deposited on the metal layer, and a photolithography process is performed by a first mask (not shown), thereby selectively forming a gate line, a line of storage region, and a gate pattern 2 of gate pad region on the substrate 1.

As shown in Figure 1B, a gate insulating layer 3, a active layer consisting of semiconductor layer, and a high-concentrated impurity layer are sequentially formed on the resulting material. Then, a photolithography is performed by a second mask (not shown) thus to selectively etch so that an active region 4 can be formed on the channel region. Herein, the active regoin 4 is formed by stacking an

amorphous silicon (a-Si) and an ohmic contact layer that a high-concentrated impurity is doped at a semiconductor layer.

The gate insulating layer and the active layer are generally deposited by a plasma enhanced chemical vapor deposition (PECVD) method.

As shown in Figure 1C, a source/drain electrode material is formed on the resulting material. Then, a photolithography is performed by a third mask (not shown) thus to selectively etch so that the source/drain material can be separated from each other at both sides of the active region 4 at the channel region. And the source/drain material can be applied as one electrode 7 of a capacitor on the gate insulating layer 3 at the storage region, and so that the source/drain material can be applied as a data electrode 8 on the gate insulating layer 3 of a data pad portion too.

As shown in Figure 1D, a passivation layer 9 is formed on the resulting material. Then, a contact hole is formed by a fourth mask (not shown) so that the drain region 6 of the channel region, the electrode 7 of the storage region, a gate pattern 2 of the gate pad portion, and the data electrode 8 of the data pad portion can be exposed.

As shown in Figure 1E, an electrode material is formed on the resulting material. Then, a photolithography is performed by a fifth mask (not shown) thus to form a pixel electrode 10 connecting the drain region 6 of the channel region and the electrode 7 of the storage region. At this time, a gate line and a data line are simultaneously formed on the gate pad portion and the data pad portion.

The aforementioned method for manufacturing an LCD device by using 5-mask has a limitation to reduce a manufacturing cost and to simplify processes due to the performance of the photolithography.

In order to solve said problem, a manufacturing method of an LCD device using 4-mask was proposed.

Hereinafter, a manufacturing process of an LCD device using 4-mask will be explained with reference to Figures 2A to 2G.

As shown in Figure 2A, a gate electrode material is formed on a glass substrate 21. Then, a

photolithography process is performed by a first mask (not shown), thereby selectively forming a gate line, a line of storage region, and an electrode pattern 22 on the substrate 21.

As shown in Figure 2B, a gate insulating layer 23, an active layer 24, and a conductive layer 25 of a metal are sequentially formed on the resulting material. Herein, the active layer 24 is a stacked layer of a semiconductor layer and a high-concentrated impurity layer.

As shown in Figure 2C, a photoresist layer(not shown) is formed on the conductive layer 25. Then, a photolithography is performed by a second mask (not shown) thus to form a pattern of the photoresist layer 40 remaining on the channel region, the storage region, and a data pad portion. On the conductive layer 25 at the channel region, a stepped photoresist pattern is formed by applying a diffraction exposure to the photoresist layer 40. A source/drain electrode and a channel are formed by applying the stepped photoresist pattern as a mask.

Figure 2D shows that the conductive layer and the active layer of regions that the photoresist pattern is not formed are etched thus to be removed by applying the photoresist layer 40 pattern as a mask.

As shown in Figure 2E, the diffraction-exposed photoresist pattern is partially removed by an ashing process, and the conductive layer above the channel region is exposed.

Thereafter, the photoresist layer 40 pattern is selectively removed thus to etch the exposed electrode layer 25 above the channel region. Next, the active layer 24 is etched with a predetermined thickness thus to form source/drain electrodes 26 and 27 separated from each other at both sides on the active layer 24, and then, as shown in Figure 2F, the remaining photoresist layer 40 pattern is removed.

As shown in Figure 2G, a passivation layer 28 is formed on the entire resulting material. Then, a photolithography is performed by a third mask (not shown) thus to selectively etch so that the drain electrode 27 of the channel region, the electrode layer 25 of the storage region, the gate pattern 22 of the gate pad portion, and the electrode layer 25 of the data pad portion can be exposed.

As shown in Figure 2H, an electrode material is formed on the resulting material. Then, a photolithography process is performed by a fourth mask (not shown) thus to selectively etch so that a

pixel electrode 29 connecting the drain region 27 of the channel region and the electrode layer 25 of the storage region can be formed and a line 30 connected to the gate pattern 22 of the gate pad portion and a line 31 connected to the electrode layer 25 of the data pad portion can be simultaneously formed.

In said manufacturing method of an LCD device using 4-mask and a photolithography, a manufacturing cost can be reduced and processes can be simplified compared to the manufacturing method of an LCD device using 5-mask.

That is, minimizing the number of masks contributes to reduce a manufacturing cost and to simplify processes.

However, efforts to reduce the number of masks in the manufacturing process of an LCD device are being variously performed. The present invention is to propose a manufacturing method of an LCD device in which the number of masks is more decreased compared to the conventional art.

[Technical object of the present Invention]

Therefore, an object of the present invention is to provide a manufacturing method of an LCD device capable of more reducing the number of mask processes than 5-mask or 4-mask generally used at the time of manufacturing a thin film transistor of an LCD device and thereby capable of simplifying processes, reducing a manufacturing cost, and enhancing a yield.

[Composition of the present Invention]

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein, there is provided a manufacturing method of a thin film transistor using 3-mask comprising: forming a gate electrode on a substrate; sequentially forming a gate insulating layer and an active layer on the gate electrode; depositing a photoresist on the active layer and performing a photolithography process thus to form a first photoresist pattern, and then removing the active layer formed at a source/drain region; ashing the first photoresist pattern thus to expose a part of an active region; forming a source/drain electrode at the source/drain region; forming a passivation layer on the substrate including the source/drain electrode; forming a second photoresist

pattern exposing a pixel region on the passivation layer; forming a pixel region by using the second photoresist pattern as a mask; side-etching a part of the passivation layer thus to expose a part of the drain electrode; forming a pixel electrode material on the second photoresist pattern and the pixel region; and simultaneously removing the second photoresist pattern and the pixel electrode material formed thereon thus to form a pixel electrode.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

[Detailed description of the preferred embodiments]

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

A manufacturing process of an LCD device according to the present invention will be explained with reference to Figures 3A to 3J.

As shown in Figure 3A, a metal layer forming a gate electrode is deposited on a substrate 300 by a sputtering method. The sputtering method is a method to deposit a target material, which is formed by colliding of target and accelerated and ionized particles on a substrate.

A photoresist is deposited on the metal layer to form a gate electrode. Then, a gate electrode 301 is formed by a photolithography process by using the photoresist as a first mask.

Then, as shown in Figure 3B, a gate insulating layer 302, an amorphous silicon layer 303, and a high-concentrated impurity layer 304 are sequentially formed on the gate electrode 301. Next, a photoresist 305 is deposited on the resulting material, and exposed and developed, thereby defining a source/drain region.

The source/drain region is defined in the present invention by removing a photoresist layer of a source/drain region and remaining a photoresist layer of the rest region.

The photoresist layer can be selectively used between a positive one or a negative one.

As shown in Figure 3C, at the substrate from which the conductive layer 304 is exposed to outside accordingly as the photoresist layer of the source/drain region is removed, the high-concentrated impurity layer 304 and the amorphous silicon layer 303 existing at the source/drain region are etched thus to be removed.

As the etching result, the photoresist 305 remains at regions including a channel region except the source/drain region. In order to form the source/drain electrode connected to the channel region, a photoresist formed at the edge of the channel region has to be partially removed.

Figure 3D shows that a part of the photoresist 305 is removed by being oxidized under an oxygen atmosphere. As the result, an entire volume of the photoresist 305 is decreased and a part of the edge of the channel region is exposed.

The process for oxidizing the photoresist 305 under the oxygen atmosphere is called as an ashing process. The ashing process is a process for removing materials reacted to an oxidation by injecting oxygen-including gas into a chamber. Referring to Figure 3D, an ashing time, a temperature, and etc. are controlled in order to partially remove the photoresist 305, thereby exposing a part of the edge of the channel region.

Next, a conductive layer 306 is formed on the resulting material of Figure 3D by a sputtering method.

Figure 3E shows the conductive layer 306 formed on the photoresist 305 formed by ashing process.

Next, a lift off process is applied so as to simultaneously remove the photoresist 305 and the conductive layer 306 formed thereon.

That is, when the lift off process is applied to the resulting material of Figure 3E, the photoresist 305 and the conductive layer 306 formed thereon are simultaneously removed and only the source/drain electrode pattern remains.

The lift off process is a process that a metal layer is formed on a photoresist pattern, then, the

photoresist is removed by a strip process and at the same time a conductive layer formed on the photoresist pattern is lifted off at one time.

Figure 3F shows a source 306a/drain 306b electrode formed by simultaneously removing the photoresist 305 and the conductive layer 306 formed thereon by the lift off process and then removing the exposed high-concentrated impurity layer.

As shown in Figure 3G, a passivation layer 307 is formed on the source/drain electrode formed by the lift off process. A photoresist is deposited on the passivation layer, and then a photoresist layer is patterned so that the photoresist can remain on the active region by using a third mask. As the result, the photoresist pattern 308 is formed above a region that a thin film transistor is formed.

Next, an etching process is performed by using the photoresist 308 of Figure 3G as a mask, thereby removing the semiconductor layer 303, and the passivation layer 307 existing on a pixel region. In order to improve an aperture ratio, the gate insulating layer 302 formed on the pixel region is further etched thus to be removed. As the result, the substrate existing at the pixel region is exposed. However, since the gate insulating layer is generally a transparent inorganic layer, it is possible not to remove the gate insulating layer.

Next, a pixel electrode material is deposited. Herein, the pixel electrode material has to be electrically connected to the drain electrode 306b. So as to expose a part of the drain electrode 306b, the passivation layer 307 is side-etched by using fluorine-including gas. When the drain electrode 306b is to be electrically connected to the pixel electrode, it is sufficient to expose the drain electrode within a range of approximately 1μm.

Figure 3H shows the passivation layer 307 that has undergone the side etching by fluorine-based gas and an aspect that a part of the drain electrode is exposed.

Referring to Figure 3H, an active layer 303b remains at one side of the source electrode. Due to the active layer 303b remaining at one side of the source electrode, the data line and the pixel electrode are excessively adjacent to each other, thereby causing a cross-talk by an interactive interference when information is inputted.

Therefore, in the present invention, the active layer remaining at one side of the source electrode that may cause the cross talk is side-etched by etching chlorine-based gas thus to be removed.

In order to prevent the cross talk between the source electrode and the pixel electrode, the active layer remaining at one side of the source electrode is etched with a range of approximately 3μm. In Figure 3I, the k region shows the active layer that has undergone the side etching.

In said process, the side etching of the passivation layer for exposing a part of the drain electrode and the side etching of the active layer for preventing the cross talk between the source electrode and the pixel electrode can be performed at the same time or at different time.

Figure 3I shows that a pixel electrode material 309 is deposited on the resulting material after performing the side etching of the passivation layer. The pixel electrode material 309 is deposited on the photoresist pattern 308 above a region that a TFT is to be formed and on the pixel region. Herein, since a part of the pixel electrode material is formed on the drain electrode exposed by the side etching, too, the drain electrode and the pixel electrode are electrically connected to each other.

As the pixel electrode material, indium tin oxide (ITO) or indium zinc oxide (IZO) having an excellent conductivity and optical transmissivity can be used.

Next, the photoresist pattern above the region that a TFT is to be formed and the pixel electrode material on the photoresist pattern are simultaneously removed by the lift off process. As the result, an LCD device including a pixel electrode 309a connected to the drain electrode is completed.

Figure 3J shows a TFT that has been completed by removing the photoresist pattern above a region that a TFT is to be formed and the pixel electrode material on the photoresist pattern by the lift off process.

[Effect of the Invention]

In the present invention, the first mask is used to form the gate pattern at the time of forming the gate electrode pattern, the second mask is used to pattern the source/drain region, and the third mask is used to form the pixel region, thereby manufacturing the TFT. According to this, the number of masks

for manufacturing the TFT is reduced thus to simplify processes. Also, a slit mask used at the conventional 4-mask process is not used thus to greatly reduce a mask cost.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalence of such metes and bounds are therefore intended to be embraced by the appended claims.

[What is claimed is]

1. A manufacturing method of a liquid crystal display device comprising:

forming a gate electrode on a substrate;

consecutively forming a gate insulating layer and an active layer on the gate electrode;

depositing a photoresist on the active layer and performing a photolithography process thus to form a first photoresist pattern, and then removing an active layer formed at a source/drain region;

ashing the first photoresist pattern thus to expose a part of an active region;

forming a source/drain electrode at the source/drain region;

forming a passivation layer on the substrate including the source/drain electrode;

forming a second photoresist pattern that exposes a pixel region on the passivation layer;

forming a pixel region by using the second photoresist pattern as a mask;

side-etching a part of the passivation layer thus to expose a part of the drain electrode;

forming a pixel electrode material on the second photoresist pattern and the pixel region; and

simultaneously removing the second photoresist pattern and the pixel electrode material formed thereon thus to form a pixel electrode.

2. The method of claim 1, wherein the step of removing the active layer formed at the source/drain region comprises:

depositing a photoresist on the active layer;

applying a mask to the photoresist, exposing, developing, and thereby forming a photoresist pattern where the source/drain region is defined; and

applying the photoresist pattern as a mask and thereby removing the active layer formed at the

source/drain region.

3. The method of claim 1, wherein the step for forming the active layer comprises:

forming a semiconductor layer on the gate insulating layer; and

forming a high-concentrated impurity layer on the semiconductor layer.

4. The method of claim 1, wherein the step for forming the source/drain electrode at the source/drain region comprises:

forming a conductive layer on the photoresist pattern where the source/drain region is defined;

simultaneously removing the photoresist pattern and the conductive layer formed thereon by a lift-off process; and

removing the high-concentrated impurity layer formed above the channel region.

5. The method of claim 1, wherein in the step for side-etching a part of the passivation layer thus to expose a part of the drain electrode, the passivation layer is side-etched by using fluorine-including gas.

6. The method of claim 1, wherein the step for side-etching a part of the passivation layer thus to expose a part of the drain electrode further comprises removing a part of the active layer remaining at a side surface of the source electrode by a side-etching.

7. The method of claim 6, wherein the active layer is removed by using chlorine ion-including gas.

8. The method of claim 1, wherein the pixel electrode material and the photoresist pattern formed thereunder are simultaneously removed by a lift-off process.

9. The method of claim 1, wherein in the step for forming a pixel electrode material on the photoresist pattern and the pixel region, the pixel electrode material is formed on a part of the drain electrode.

10. The method of claim 1, wherein the step for ashing the first photoresist pattern thus to expose a part of an active region further comprises exposing a part of a high-concentrated impurity layer of the active region by oxidizing a part of the photoresist with oxygen ion-including plasma gas.

11. The method of claim 1, wherein the step for applying a second photoresist pattern as a mask thus to form a pixel region comprises sequentially removing the passivation layer and the active layer formed at the pixel region.

FIG. 1A
RELATED ART

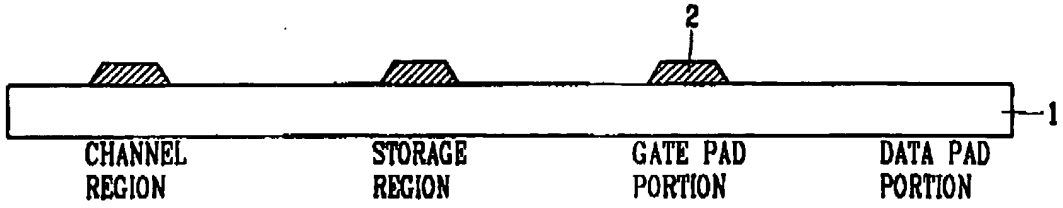

FIG. 1B
RELATED ART

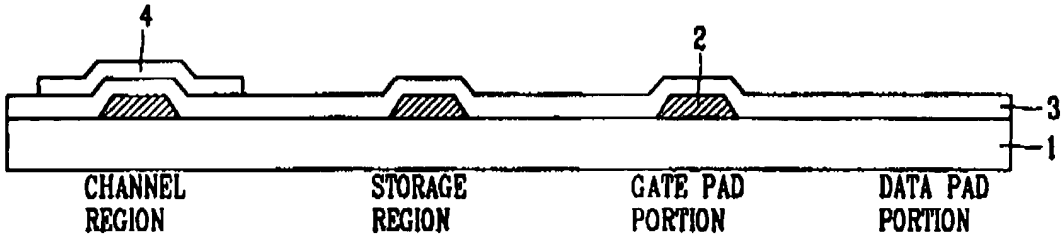

FIG. 1C
RELATED ART

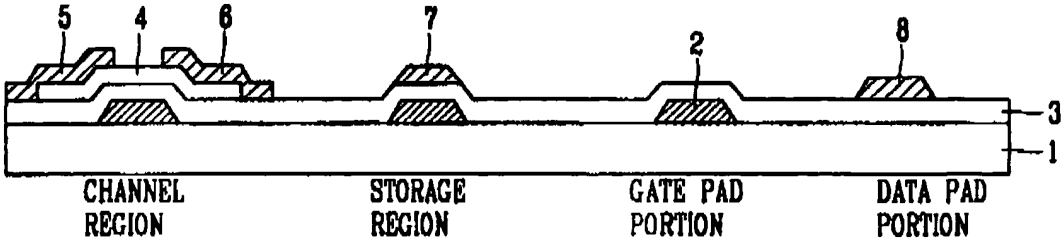

FIG. 1D
RELATED ART

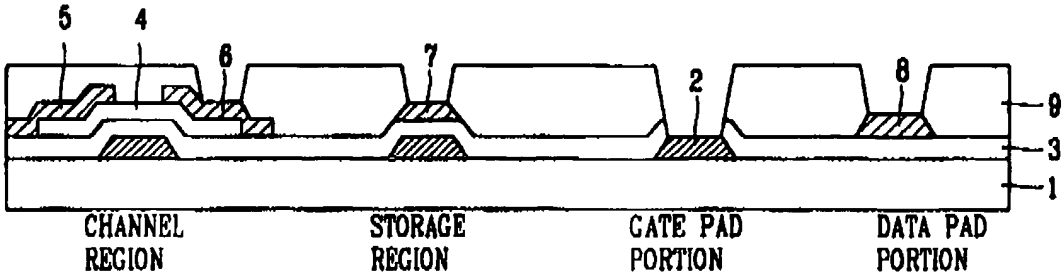

FIG. 1E
RELATED ART

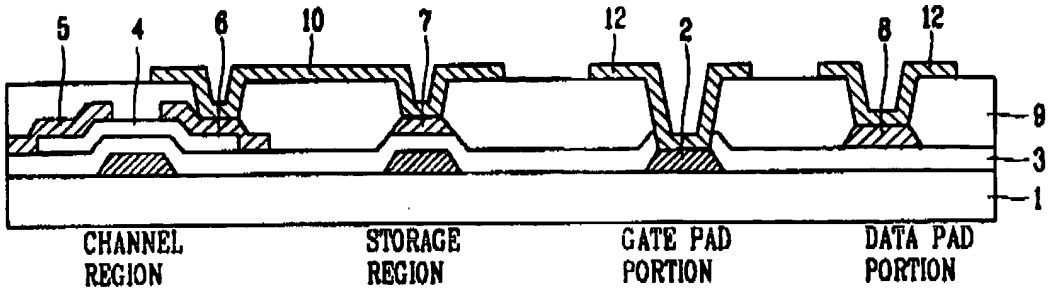

FIG. 2A
RELATED ART

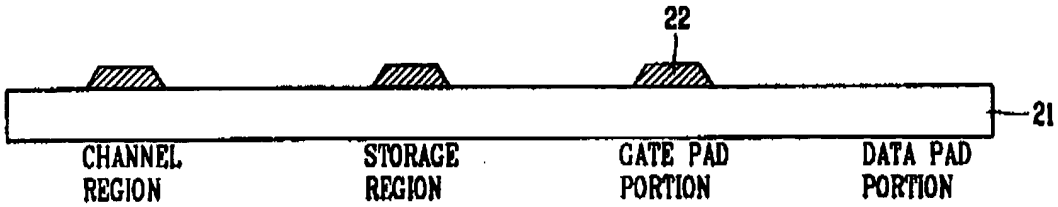

FIG. 2B
RELATED ART

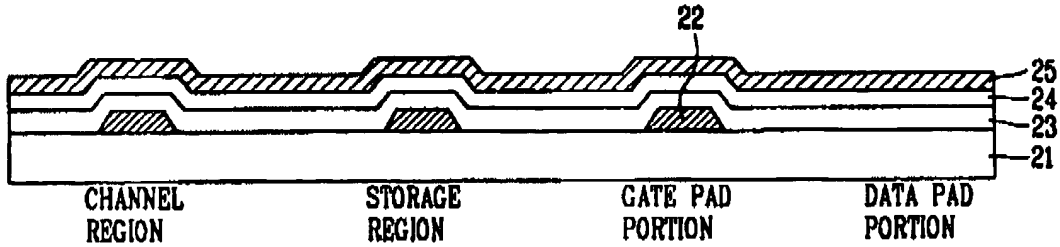

FIG. 2C
RELATED ART

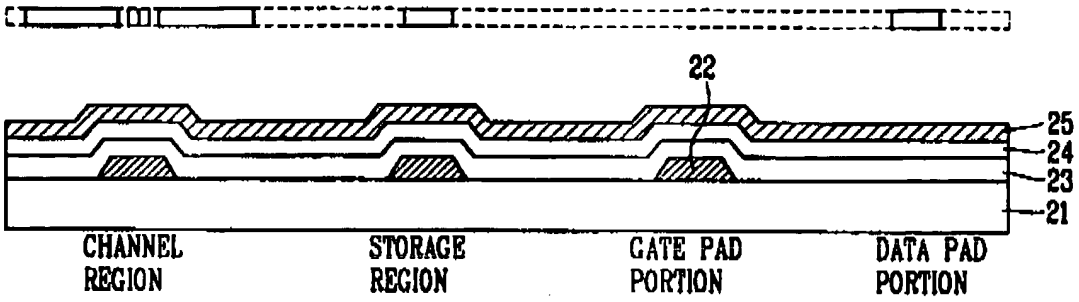

FIG. 2D
RELATED ART

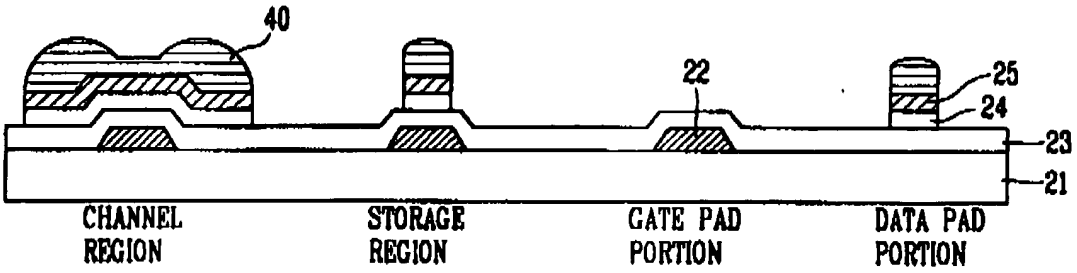

FIG. 2E
RELATED ART

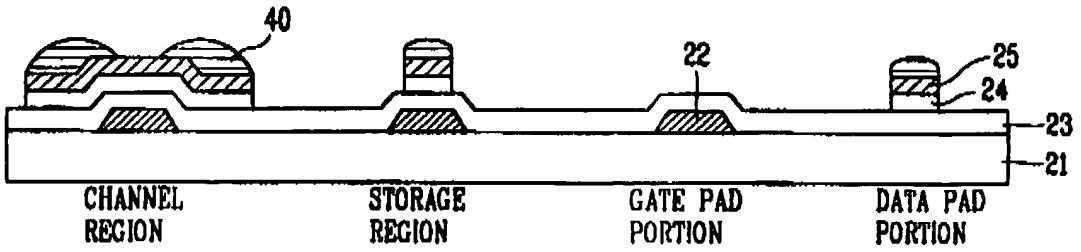

FIG. 2F
RELATED ART

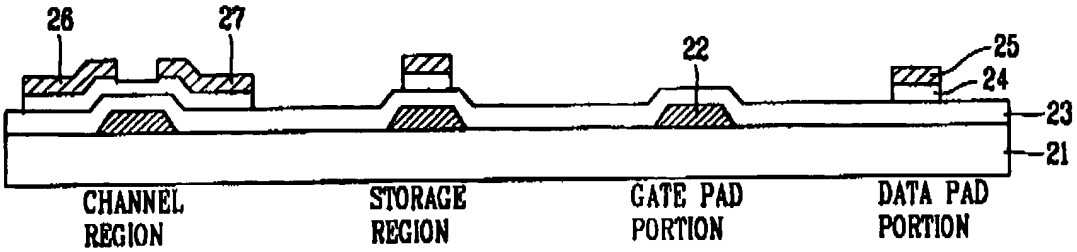

FIG. 2G
RELATED ART

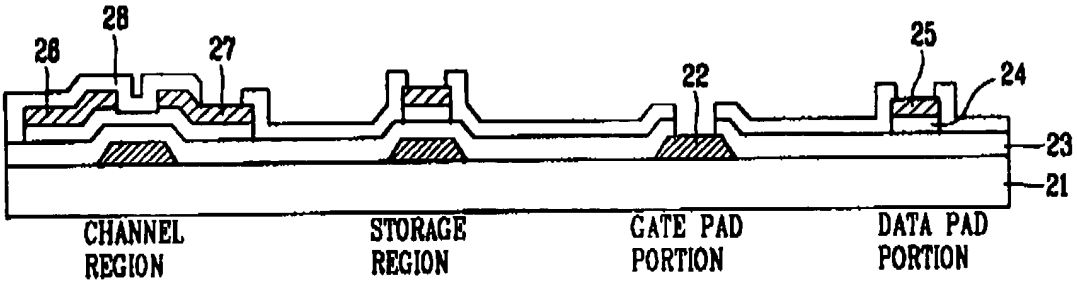

FIG. 2H
RELATED ART

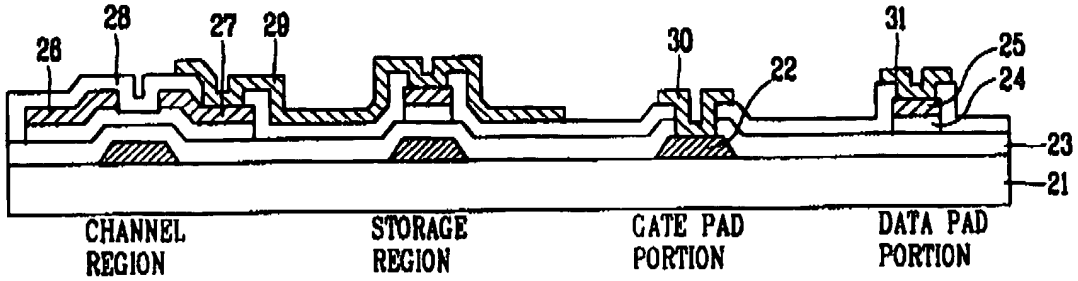

FIG. 3A

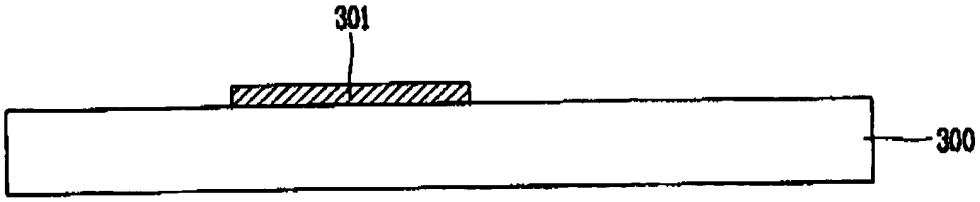

FIG. 3B

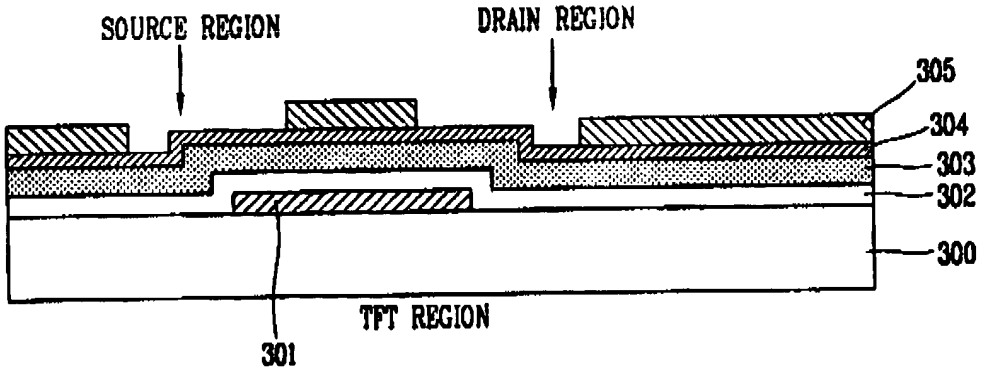

FIG. 3C

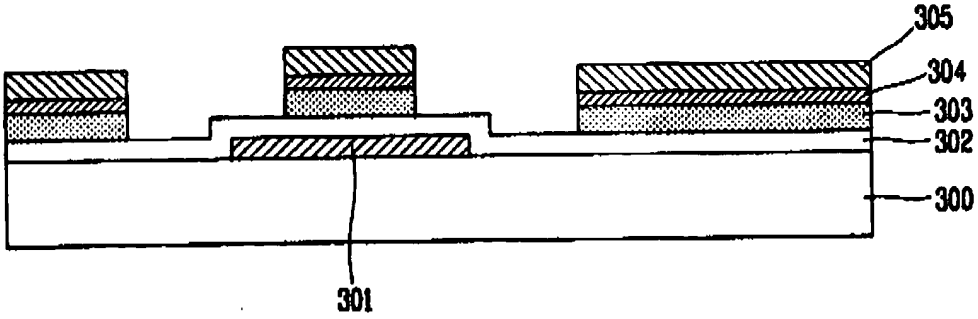

FIG. 3D

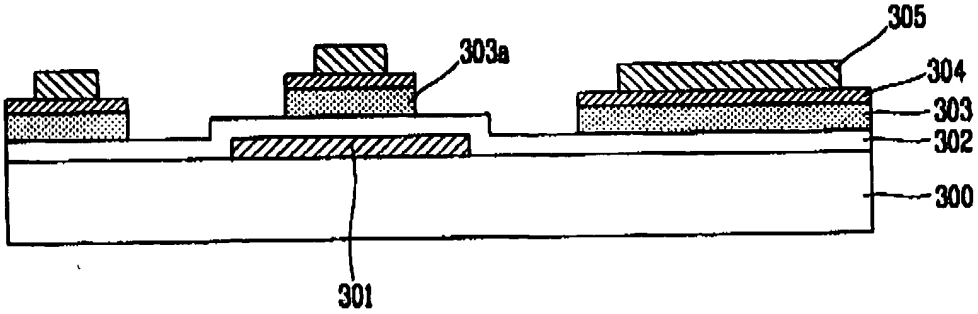

FIG. 3E

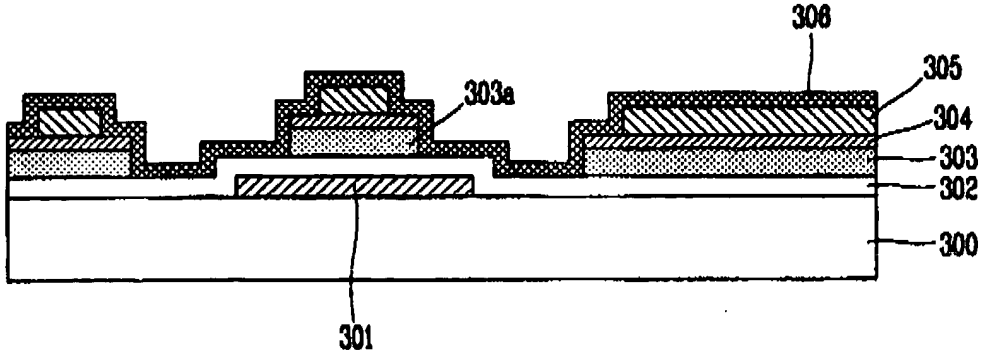

FIG. 3F

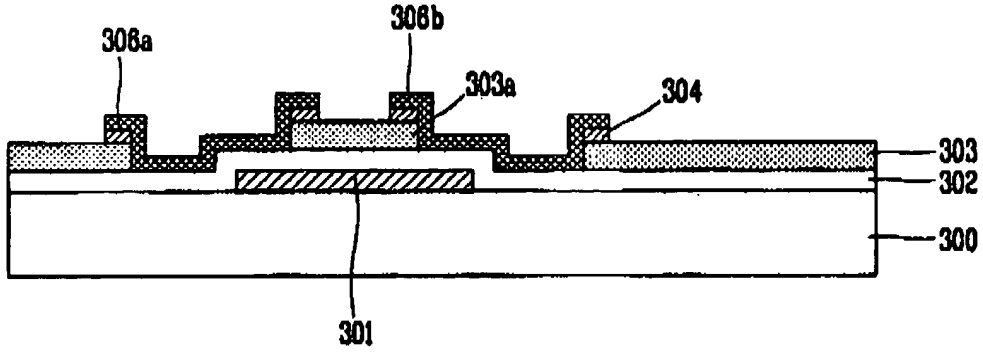

FIG. 3G

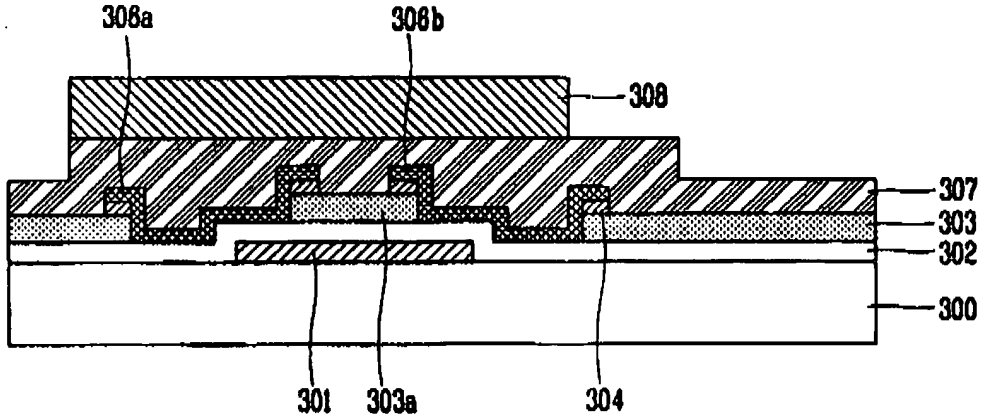

FIG. 3H

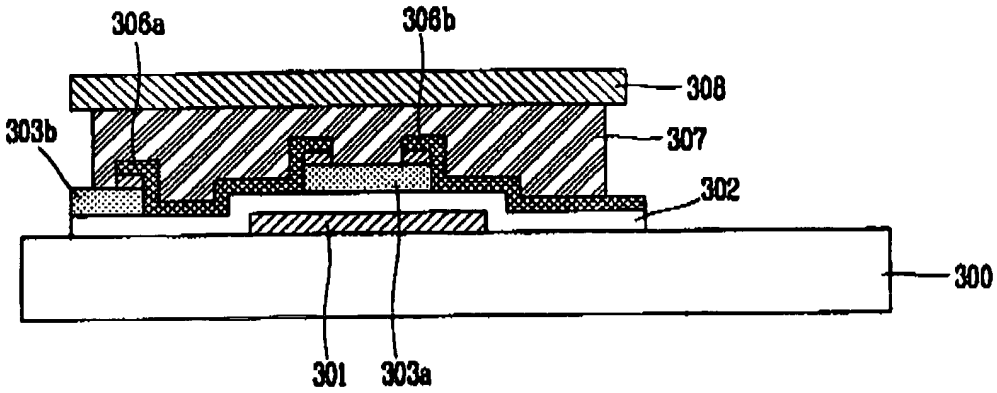

FIG. 3I

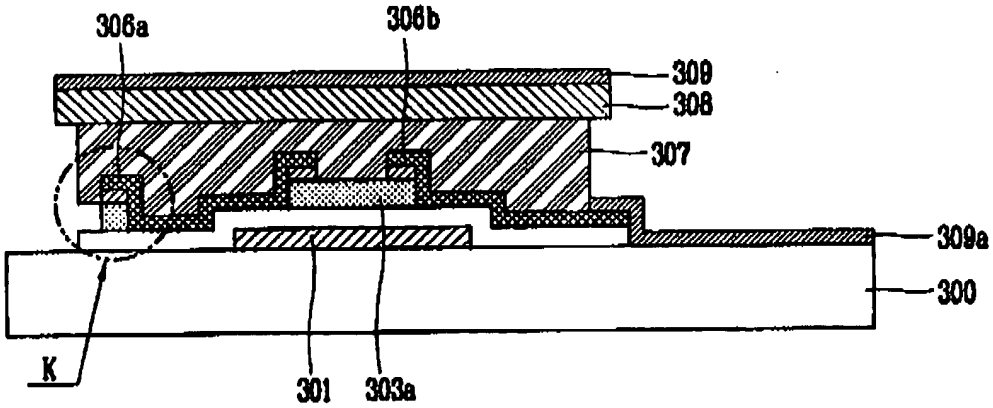

FIG. 3J